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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,814	07/13/2001	Christopher D. McBride	1662-34200 JMH (P99-2711)	4414

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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,814	MCBRIDE ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *32-39* is/are withdrawn from consideration.

5)☒ Claim(s) *1-16 and 22-31* is/are allowed.

6)☒ Claim(s) *17,18,20 and 21* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Drawings dated 3/4/02.

2. Claims 1-10, 17-28 and 30 are presented for examination.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10, 17-21, 22-28 and 30, drawn to selecting delay in a clock path between a PLL and memory controller, classified in class 713, subclass 401.

II. Claims 1, 11-16, 22, 29, and 30-39 drawn to selecting delay in the feedback path of a PLL, classified in class 713, subclass 503.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the selectable delay between a PLL and a memory controller is useable in a system that does not require selectable delay in the feedback path of the PLL. The subcombination has separate utility such as being used in system that does not have selectable

delay on the non-feedback path at the output of the PLL. In sum, the two paths are independent and each have a different effect.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Jonathan M. Harris, Reg. No. 44,144 on 19 October 2004 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-10, 17-21, 22-28 and 30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-16, 29 and 31-39 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

4. Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37

CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bogumil et al., 6,253,333 in view of Takahashi, U.S. Patent 6,370,200.

7. As to claim 17, Bogumil substantially teaches a method of adaptively compensating for parasitic capacitance on a bus transferring data from a sending to a receiving device, comprising:

a. coupling a plurality of signal paths (paths with delays 1, 2 and 3 in elements 50 and 52 of figure 1; each of the paths have a different electrical length; col. 4 lines 14-23), between a source of a read clock and the receiving device (from the clock tree to the SDRAM 20 and 22), which receiving device uses the read clock as a trigger to read data from the bus (col. 2 lines 39-53);

b. selecting on of the signal paths (using MUXes 55 and 57; figure 1), based on at least in part on the parasitic capacitance (inherent within the system due to SDRAM), by forcing an electrically controlled switch into a conduction mode (MUXes are electrically controlled switches), for the path desired, and by forcing remaining electrically controlled

switches, associated with other paths, into a nonconductive mode (only the selected path for a MUX is in a conductive mode); thereby

c. adjusting a phase relationship between the read clock and the a write clock, used by the sending device (delay control circuits 50 and 52) as a trigger to drive data to the bus (col. 2 lines 37-53).

In sum, Bogumil teaches adjusting the synchronization clock for transferring data to compensate for delay caused by among other things parasitic capacitance. Bogumil does this by selecting on of a plurality of paths for a clock signal having a specific delay.

Bogumil does not detail how the delay paths are implemented. However, Bogumil suggests to those of ordinary skill that there are many ways to implement the delay paths (col. 4 lines 14-20).

Takahashi teaches coupling a plurality of signal paths, at least two of the plurality having different path lengths (col. 5 lines 52-58 and figure 2 (b)). Takahashi teaches a system where different paths are selected to adjust for delay in the signal paths. Takahashi would suggest that using different using paths of different lengths is a simple implementation that uses less power than other implementation.

It would have been obvious to one of ordinary skill in the art, having the teachings of Bogumil and Takahashi before him at the time the invention was made, to use the delay lines taught by Takahashi for the delay lines disclosed by Bogumil as the delay lines taught by Takahashi is suitable for use as the delay lines of Bogumil.

8. As to claim 18, Bogumil together with Takahashi substantially taught the method according to claim 17. Bogumil further teaches using a multiplexer to which when forcing its electrically controlled switches into conductive and nonconductive modes further comprises asserting a first output signal of a control device coupled to a gate connection of a first FET, substantially simultaneously deasserting a second output signals of the control device coupled to a gate connection of a second FET. The multiplexer thereby passes the read clock through the first FET and one of said plurality of signal paths and preventing the passage of the read clock through the second FET thereby disallowing propagation of said read clock through remaining signal paths of the plurality of signal paths.

9. As to claim 20, Bogumil together with Takahashi substantially taught the method according to claim 18 described above. Bogumil further teaches wherein selecting one of the signal paths further comprises determining a shortest signal path length of the read clock at which data transfers between the sending device and the receiving device without error (col. 5 line 36 through col. 6 line 22). In summary, Bogumil teaches that the path with no error would be selected.

10. As to claim 21, Bogumil together with Takahashi substantially taught the method according to claim 18 described above. Bogumil teaches testing by transferring data from the sending device to the receiving device and checking it for bit errors and selecting a path length for the read clock at which no bit errors occurred in the transfer of the test data (col. 5 lines 38-44).

Bogumil together with Takahashi do not discuss testing each signal path form a longest (worst case) path length to the shortest (best case) path length said testing continued until the

signal path length for the read clock causes bit errors in the transfer of the test data. Instead Bogumil shows by way of example starting a nominal value then selecting either a longer path or a shorter path.

One of ordinary skill in the art will recognize that starting with the longest or shortest path length is not essential. The length that is finally chosen would still be the shortest possible length without errors. In sum, starting value of the path length would not change the resulting final selection of the path length.

Allowable Subject Matter

11. Claims 1-16 and 22-31 are allowed.

12. Claims 1, 22 and 30 are generic and allowable. Accordingly, the restriction requirement as to the encompassed species is hereby withdrawn and claims 11-16, 29 and 31, directed to the species of Group II is no longer withdrawn from consideration since all of the claims to this species depend from or otherwise include each of the limitations of an allowed generic claim. However, claims 32-39, directed to the species of Group II remain withdrawn from consideration since they do not all depend upon or otherwise include all the limitations of an allowed generic claim as required by 37 CFR 1.141.

In view of the above noted withdrawal of the restriction requirement as to the linked species, applicant(s) are advised that if any claim(s) depending from or including all the limitations of the allowable generic linking claim(s) be presented in a continuation or divisional application, such claims may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 44 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

13. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is an examiner's statement of reasons for allowance:

Bogumil together with Takahashi taught the claimed method as set forth hereinabove.

Hofstra, U.S. Pat. No. 6,535,038 teaches using different path lengths to compensate for clock skew in clock paths to a memory array (figures 4 and 5).

Lee, U.S. Pat. No. 6,530,001 teaches in figure 3 and in the corresponding text a computer system having a microprocessor (CPU) coupled to a primary bridge (Host to PCI bridge 120). Lee also shows in figure 3 a main memory (memory 20) coupled to a memory controller (32) by way of a memory bus, said memory controller integral with said primary bridge device (32 is part of controller 30). Figure 3 of Lee further discloses a secondary bridge (PSA to ISA bus bridge) coupled to a said primary bridge device by way of a primary expansion bus (PCI bus). As depicted in figure 3, Lee further has an input/output controller (I/O controller 90) coupled to the second bridge device by way of secondary expansion bus. Lee also shows a read only memory (Bios ROM 50 and CD-ROM 72) coupled to the secondary bridge by way of the secondary expansion bus, said ROM stores programs executable by the microprocessor (inherent) in figure 3. Lee shows a keyboard (keyboard 92) coupled to said input/output controller and a host clock generator having a host clock signal coupled to the memory controller in figure 3. The host clock of Lee generates a plurality of clock signals (components BXCLK and BXPCLK; col. 7, lines 45-55). Lee does not describe the detail how the host clock is generated. Those of ordinary skill understand and appreciate how PLL operate and would be implemented to generate a host clock. Those of ordinary skill in the art also know PLLs are widely used because they generate a stable clock output. Even though Lee does not show a PLL it would have been obvious to one of ordinary skill in the art to implement a PLL to generate the host clock of Lee because PLLs provide stable clock outputs.

Dixon, U.S. Pat. No. 6,496,911 teaches determine the number of memory modules to determine the amount of drive required to properly drive the memory module (col. 7 lines 17-20).

Matsuzaki, U.S. Pat. No. 6,194,930. This patent teaches a DLL circuit that has variable delay on its output path.

U.S. Pat. No. 6,513,135 to Dell. This patent teaches SDRAMs and DRAMs comprising of DIMMs.

Neil H. E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley Publishing Company, Second Edition, Page(s): 17-18. This excerpt teaches how multiplexers are implement using field effect transistors.

Applicant's admitted prior teaches how parasitic capacitance affects clock signals and data transfer in a computer system

However, the prior art of record fails to teach or even suggest either individually or in combination the structure of a delay circuit coupled between PLL output signal and a memory controller as per claims 1, 22, and 30. The prior art of record also fails to teach or even suggest either individually or in combination determining the number of memory modules in a sending device and referring to a look-up table that directs the use of the one of said signal path based on the number of memory modules.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
October 27, 2004

REHANA PERVEEN
PRIMARY EXAMINER